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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,004	02/08/2002	Woo Young So	1514.1010	6442

21171 7590 07/13/2004

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,004	SO ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-16 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-16 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948).
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/16/2004 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda et al. ("Yoneda") USPN 5,837,568 in view of Yamazaki et al. ("Yamazaki") USPN 5,568,288.

Yoneda discloses in figs. 12 and 13 a thin film transistor (TFT), comprising: a substrate 10; a semiconductor layer formed over said substrate having end portions; a first insulating layer 12 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer; a gate electrode 13 formed over said first insulating layer; a capping layer 14 formed over said gate electrode; spacers 15 formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions 11 formed at the ones of the

end portions of said semiconductor layer exposed beyond said spacers; source and drain electrodes 17/18 which directly contact, respectively, said high density source and drain regions, but do not disclose source and drain electrodes contacting high density source and drain regions without contact holes.

Yamazaki discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode 107 formed over an insulating layer 103; a capping layer 106 formed over said gate electrode; and source and drain electrodes 102 which directly contact, respectively, and without contact holes, said high density source and drain regions.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Yamazaki's teachings with Yoneda's device since that would prevent flickering and display failure as taught by Yamazaki.

Regarding claim 13, Yoneda discloses low-density source and drain regions 11L having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under spacers between the gate electrode and the high density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers.

Regarding claim 14, Yoneda discloses said first insulating layer, said capping layer and said spacer are of an oxide.

4. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Yamazaki.

Yoneda discloses in figs. 12 and 13 an active matrix display device, comprising: a substrate 10; a semiconductor layer having end portions formed over said substrate; a

first insulating layer 12 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 13 formed over said first insulating layer; a capping layer 14 formed over said gate electrode; spacers 15 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions 11formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; source and drain electrodes 17/18 which directly contact, respectively, said high density source and drain regions; a planarization layer 19 having an opening portion CT3 which exposes a portion of one of said source and drain electrodes; and a pixel electrode 20 formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion, but do not disclose source and drain electrodes contacting high density source and drain regions without contact holes.

Yamazaki discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode 107 formed over an insulating layer 103; a capping layer 106 formed over said gate electrode; and source and drain electrodes 102 which directly contact, respectively, and without contact holes, said high density source and drain regions.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Yamazaki's teachings with Yoneda's device since that would prevent flickering and display failure as taught by Yamazaki.

Regarding claim 23, Yoneda discloses low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-

set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers.

5. Claims 15, 16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Yamazaki as applied to claims 12 and 22 above and further in view of Yamazaki et al. (JP 11-261076).

The combined references disclose the device structure as recited in the claim, but do not disclose a silicide layer.

Yamazaki et al disclose in fig. 1 a silicide layer 105a or a refractory metal (as in claim 16) formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Yamazaki et al with the device of combined references, since that would lessen the source/drain regions in sheet resistance as taught by Yamazaki et al.

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Yamazaki as applied to claim 22 above, and further in view of Tang et al. ("Tang") USPN 5,550,066.

The combined references fail to disclose an organic electro-luminescence (EL) layer and a cathode electrode.

Tang discloses an organic electro-luminescence (EL) layer 82 and a cathode electrode 84 sequentially formed on a first predetermined area of said pixel electrode and on a second predetermined area of a planarization layer 74.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Tang's teachings with the device of the combined references, since that would provide a high efficiency.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
July 11, 2004